Better Foundations for Secure Software using Trusted Hardware & Verification

Shweta Shinde ETH Zürich

Security breaches are on the rise

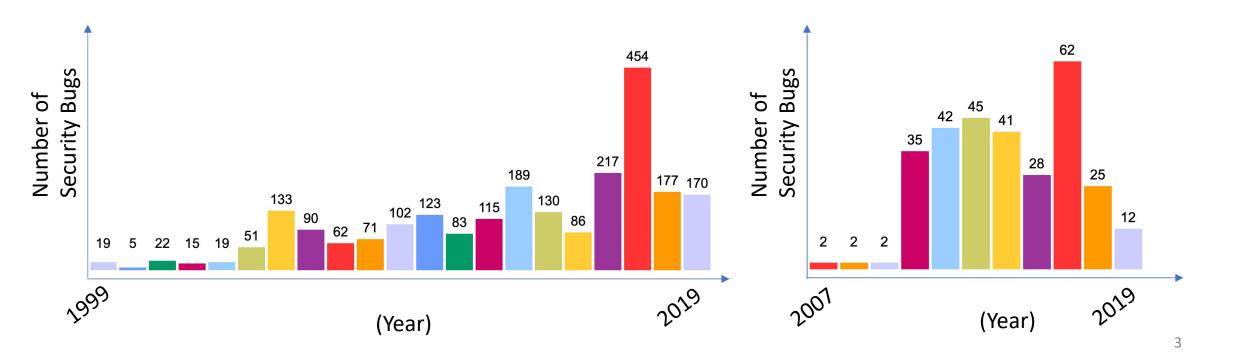
37 billion records exposed through data breaches in 2020

Average of 1-25 Bugs per 1000 lines of code

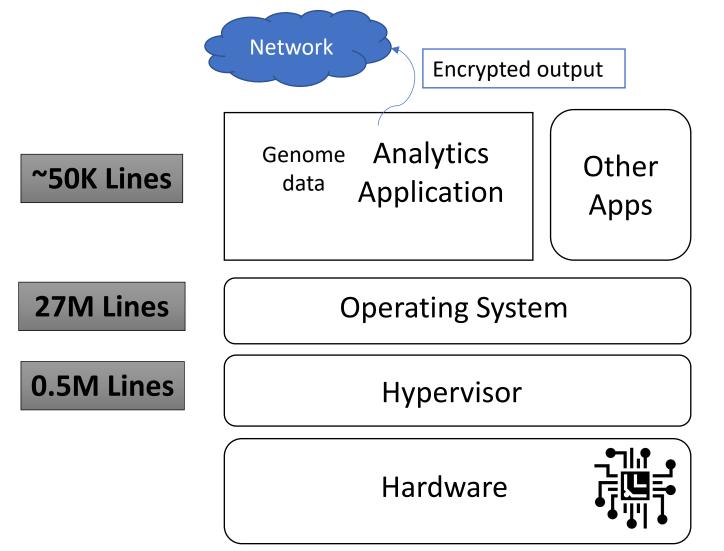
The new normal: Hundreds of bugs a year in Linux

Operating System (Linux Kernel) 27 Million Lines

Hypervisor (XEN) 0.5 Million Lines



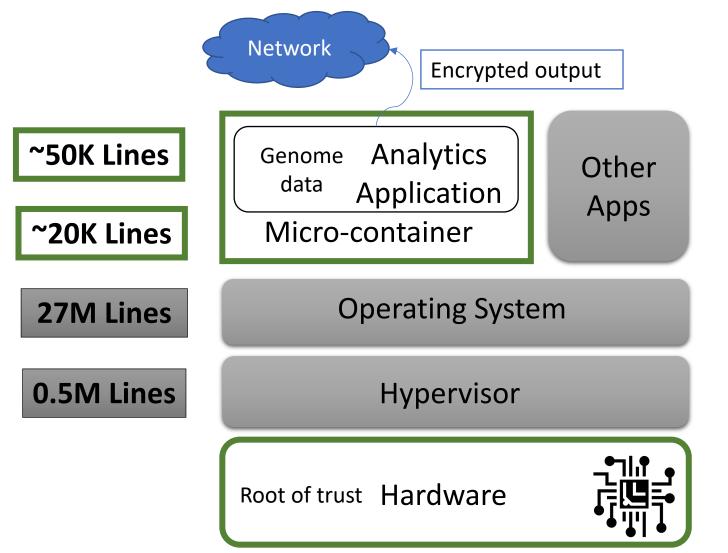
Current computing stack is prone to attacks



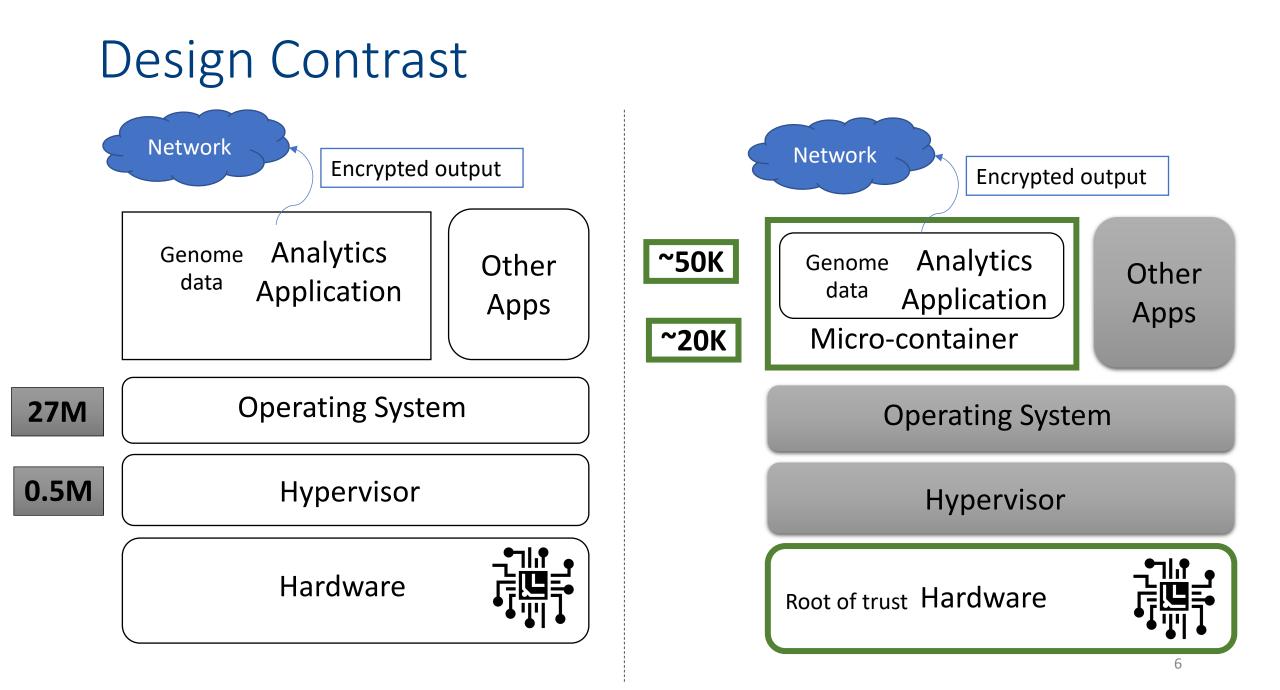
- Encryption or other sophisticated techniques at the application layer
- Bug in lower layers → Compromise the security of the app

Large size →
 High probability

Computation stack for the decades to come



- Thin layer for running applications
- Trusted hardware
- Formal guarantees for defense against
 - Third party attacks
 - Internal bugs in the app



Building the components of this stack

New Applications [Arxiv'18], [ICDCS'19] Secure Computation [CCS'13]

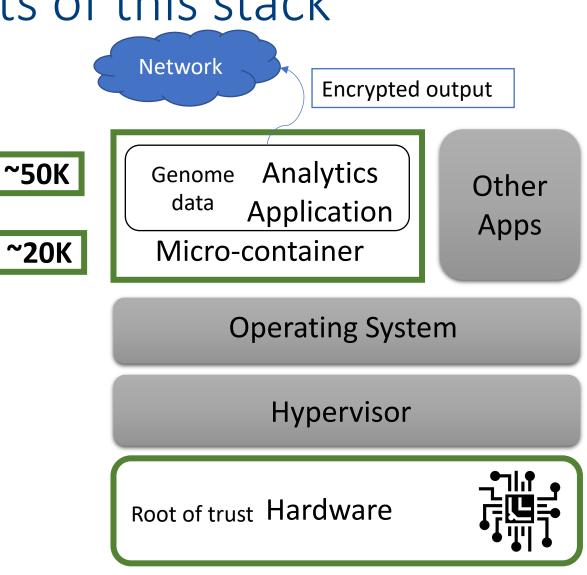
Analysis & hardening [PLDI'14], [FSE'15], [NDSS'19], [CCS'20]

Rich functionality [NDSS'17], [Usenix'22]

Formal verification [Usenix Security'20]

Attacks & Defenses [AsiaCCS'16] [CCS'21]

Trusted Computing Primitives [TR'15], [Eurosys'20]

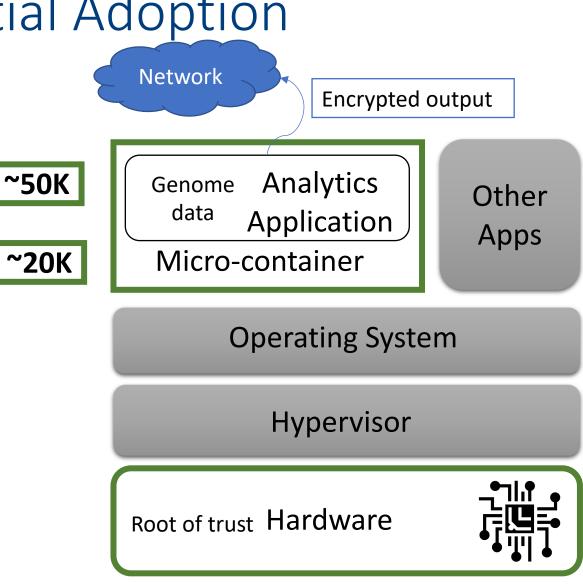


Practical Relevance: Initial Adoption

New Applications Microsoft, Largest Asia-Pacific ISP Secure Computation SAP Labs Analysis & hardening Dexecure

Rich functionality Anglave, Anguan, Community Formal verification Intel, Google, Microsoft, Anglave Attacks & Defenses Intel, Community

Trusted Computing Primitives Qualcomm, Seagate, Baidu, Community



1st Component of this stack

New Applications [Arxiv'18], [ICDCS'19] Secure Computation [CCS'13]

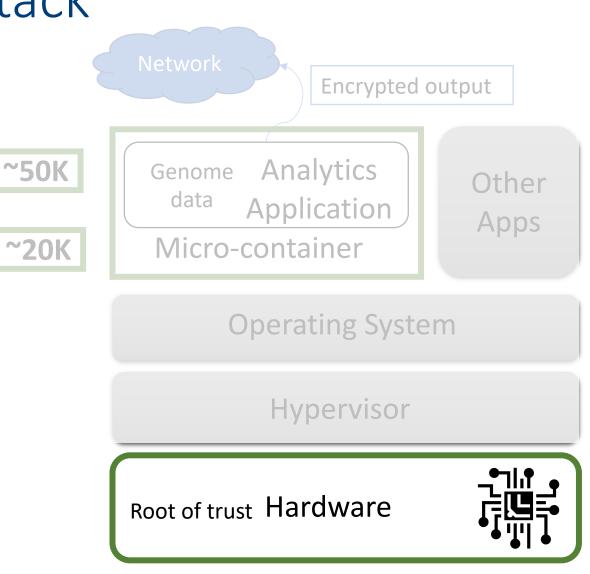
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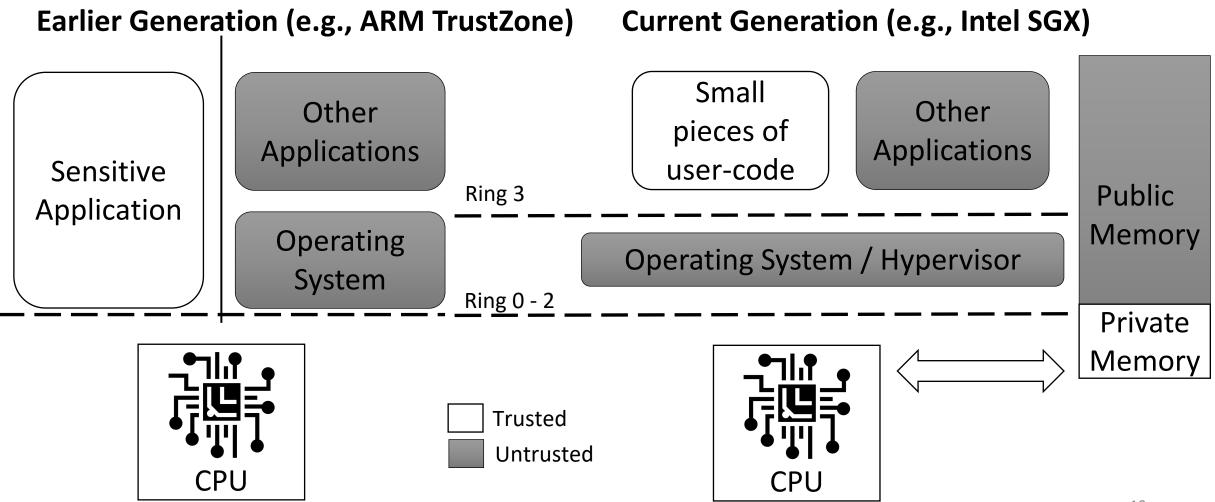
Formal verification [Usenix Security'20]

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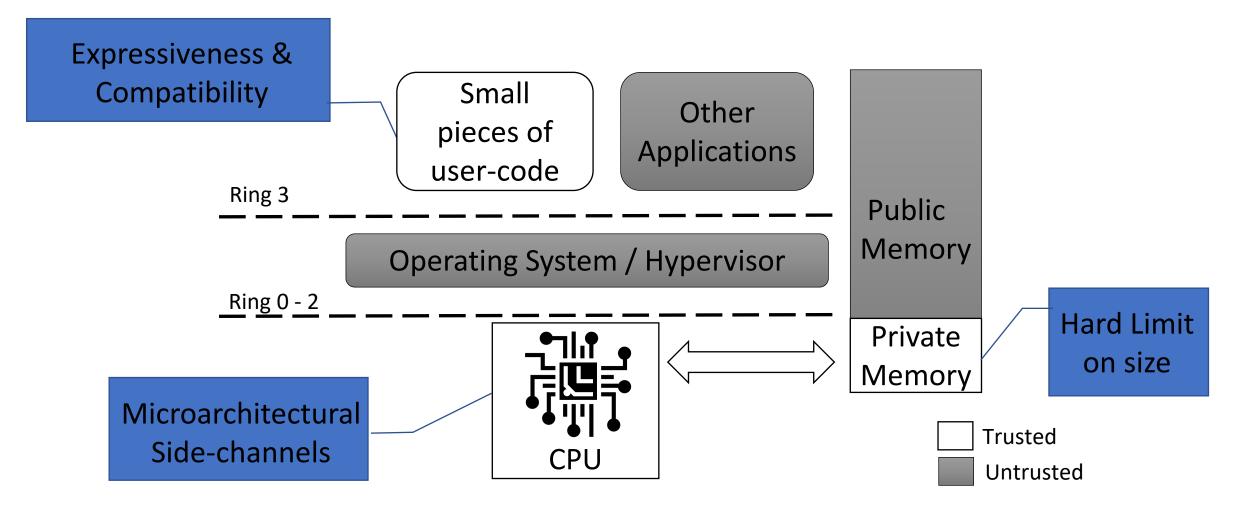
Trusted Execution Environments (TEEs)



Inflexible Design & Closed Implementation

- TEEs in commercial hardware: Intel SGX, ARM TrustZone, AMD SEV
- One particular design point in the space
 - Intel SGX small server/desktop apps (e.g., DRM, cryptography)
 - ARM TZ vendor-provisioned mobile apps (e.g., fingerprint, ledger)
 - AMD SEV full VM isolation only (e.g., cloud computing)
- Implemented on closed-source hardware
 - Slow iteration dictated by a company
 - Adding new features/defenses is cumbersome

Limitations of Commercial TEEs

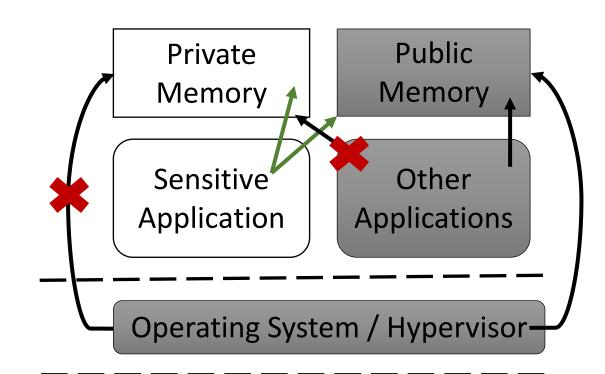


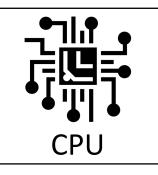
Binary Compatibility For SGX Enclaves [arXiv'20]

Better TEEs

- Main Observation:
 - Physical memory isolation
 - Simpler ways to achieve
- Similar abstraction to Intel's TEE
- Novelty: Designed to maintain
 - Compatibility
 - Performance

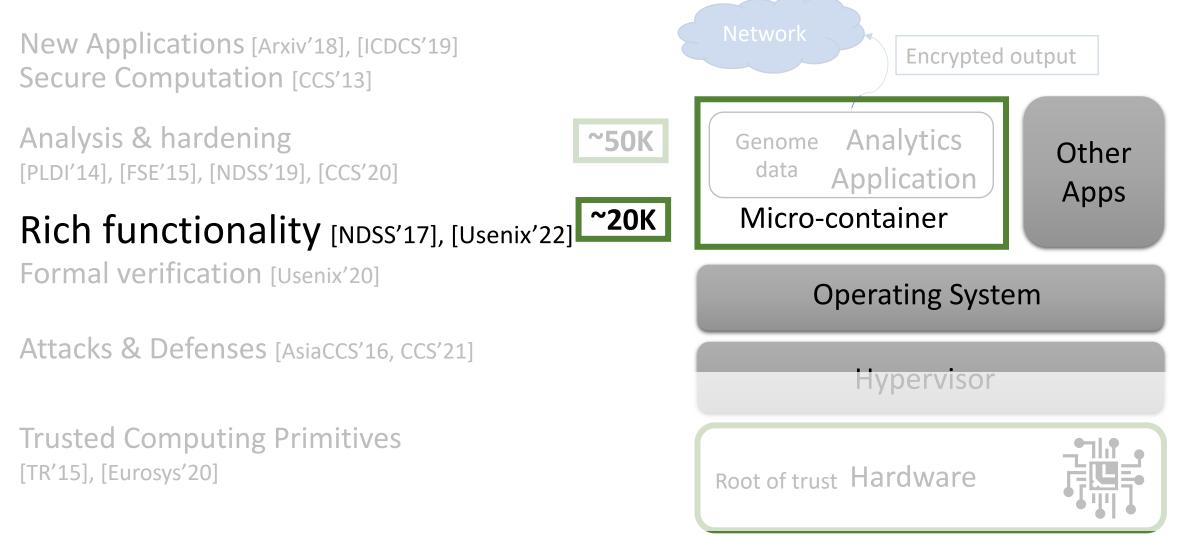




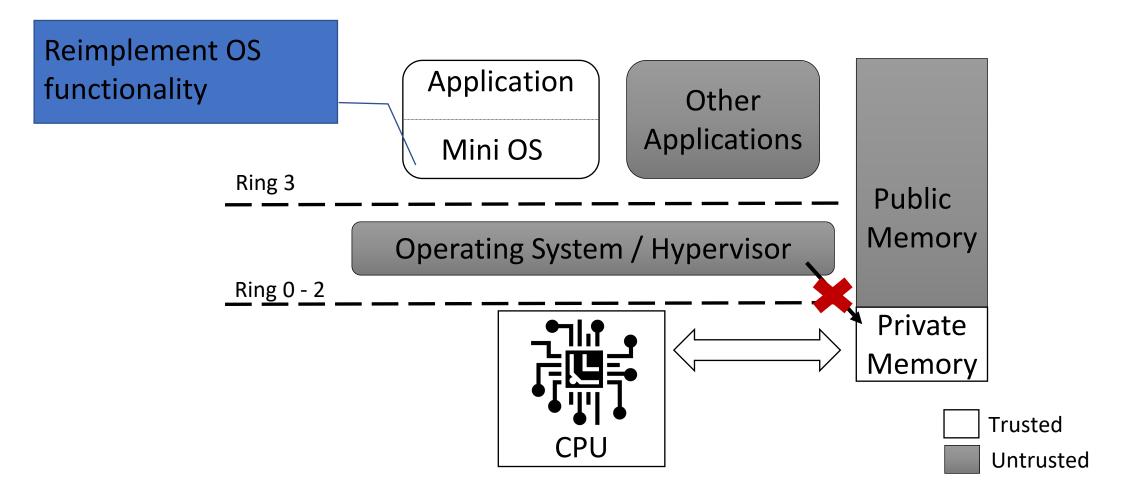


Focus on commercial TEEs (e.g., Intel SGX), since they are widely available

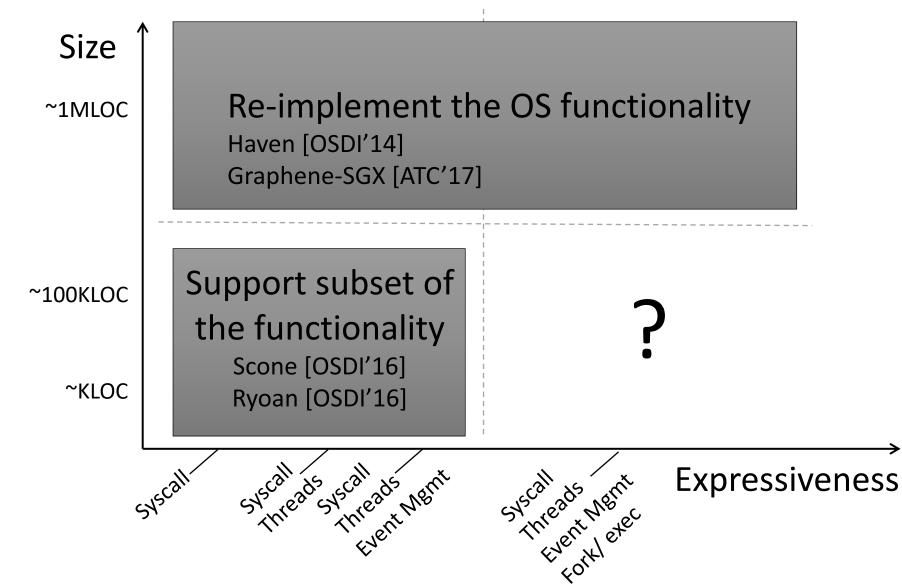
2nd component of this stack



Adding Expressiveness to Commercial TEEs

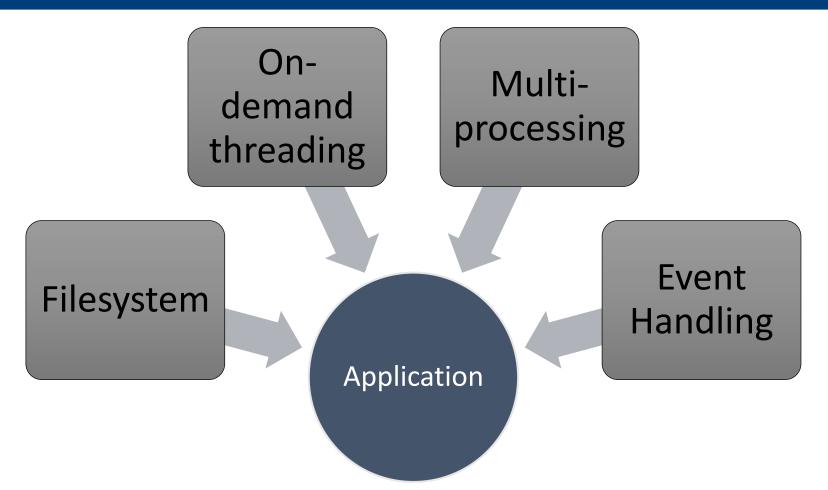


Code Size & Expressiveness Trade-off

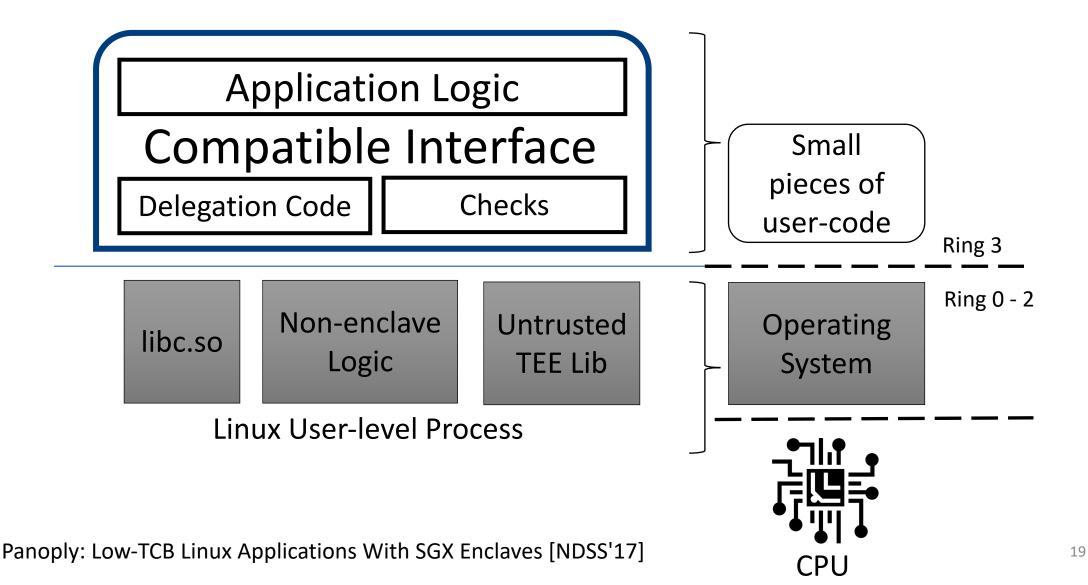


Challenge I: Expressiveness

Delegate rather than emulate

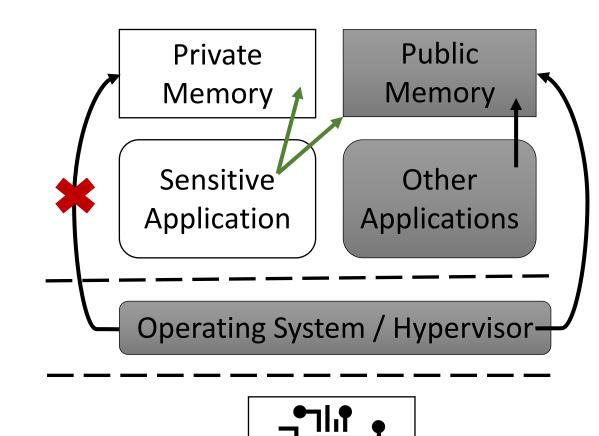


Building micro-container abstractions for TEEs



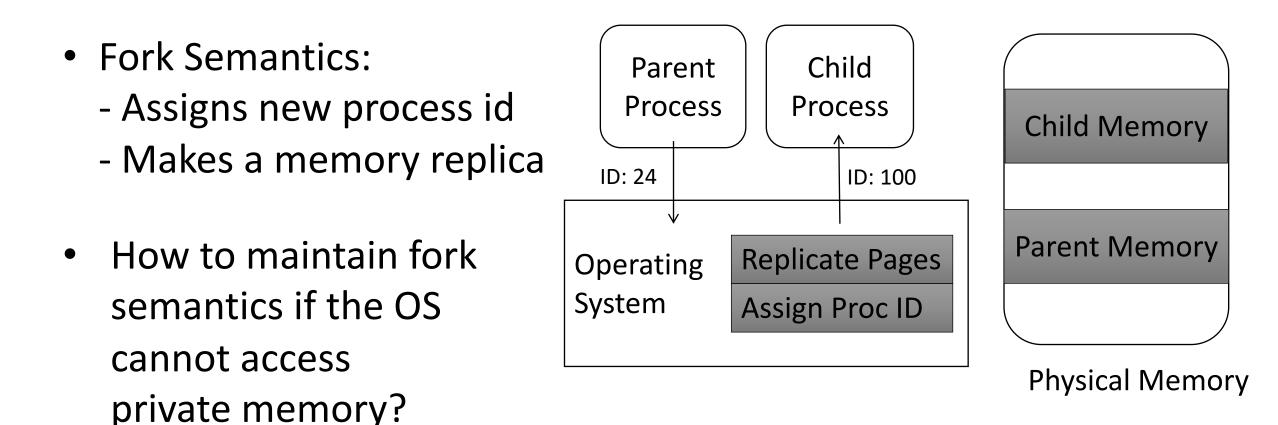
Challenge II: Delegation with isolation

- Two memory model:
 private and public memory
- Process abstraction breaks
 locks are in public memory
 - shared memory for processes
 - passing data to system calls



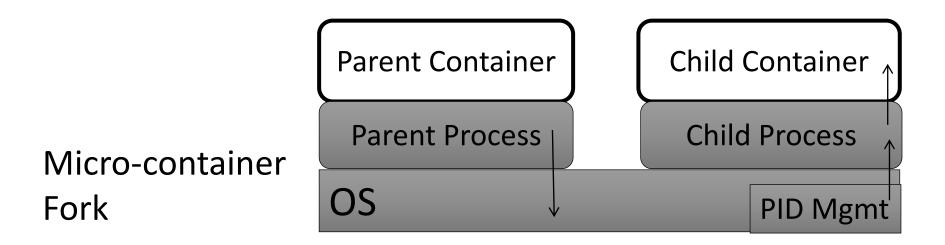
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Expressiveness Example: Fork



Expressiveness Example: Delegating Fork

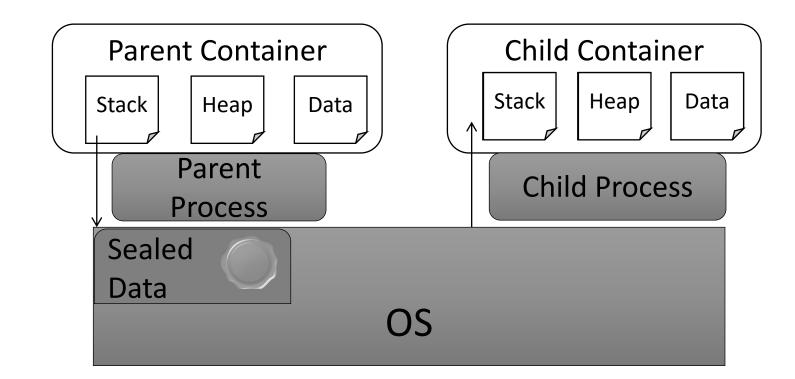
• Creating child process and child micro-container



• Child enclave has a clean memory state

Expressiveness Example: Achieving Fork Semantics

- Mirroring parent's memory in child micro-container
 - After the fork call, before resuming execution



Expressiveness: Supporting POSIX APIs

Core Services	
Process Creation and Control	5
Signals	6
Timers	5
File and Directory Operations	37
Pipes	4
C Library (Standard C)	66
I/O Port Interface and Control	40

Thread Extensions

Thread Creation, Control, and Cleanup	17
and Cleanup	
Thread Scheduling	4
Thread Synchronization	10
Signal Delivery	2
Signal Handling	3

Real-time Extensions

Real-Time Signals	4
Clocks and Timers	1
Semaphores	2
Message Passing	7
Shared Memory	6
Asynchronous and	29
Synchronous I/O	C
Memory Locking Interface	6

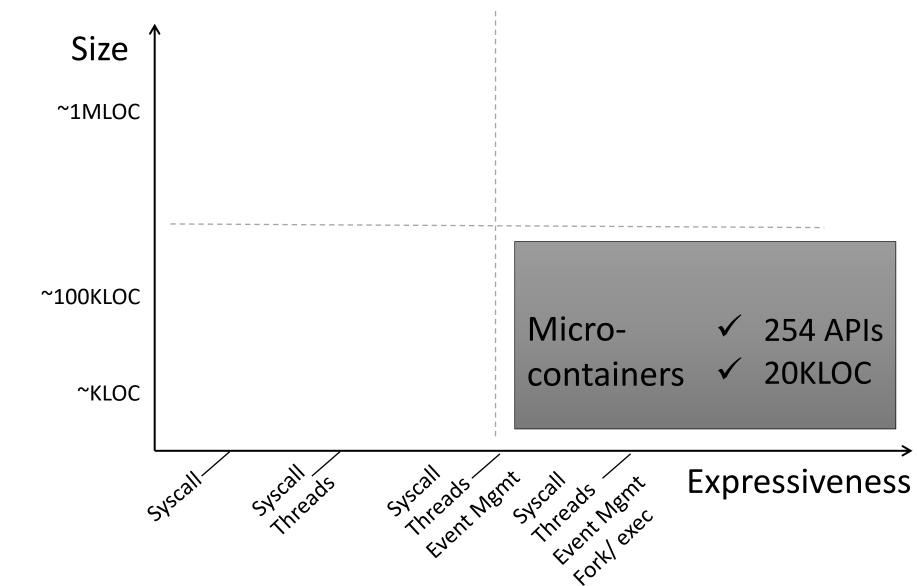
POSIX APIs Supported for Commodity Linux Apps

Micro-containers execute TEE use-cases

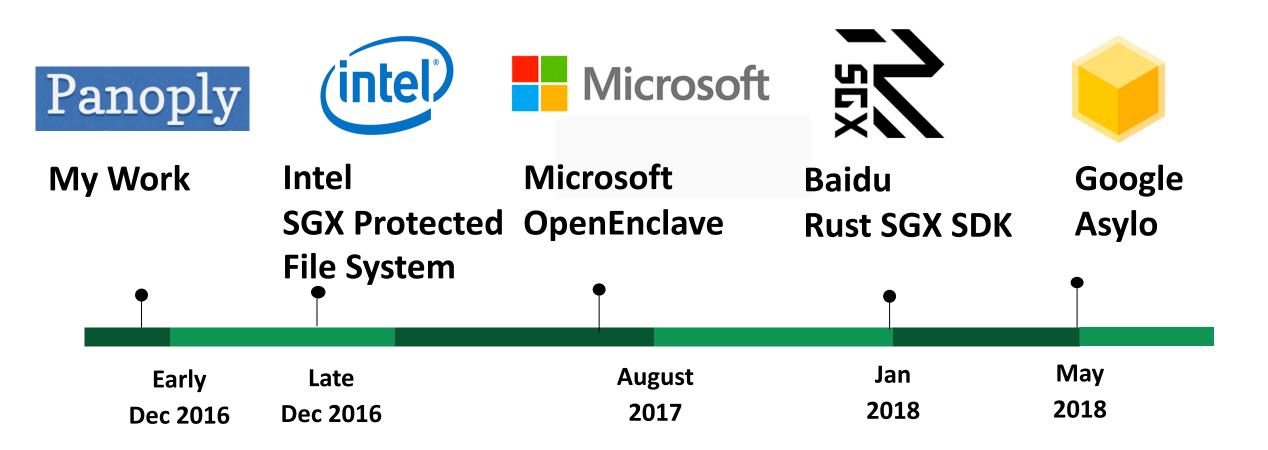


Performance is comparable to importing a mini-OS

Minimize Trust to 20,000 lines of code



Adoption of the Delegation Approach



3rd component of this stack

New Applications [Arxiv'18], [ICDCS'19] Secure Computation [CCS'13]

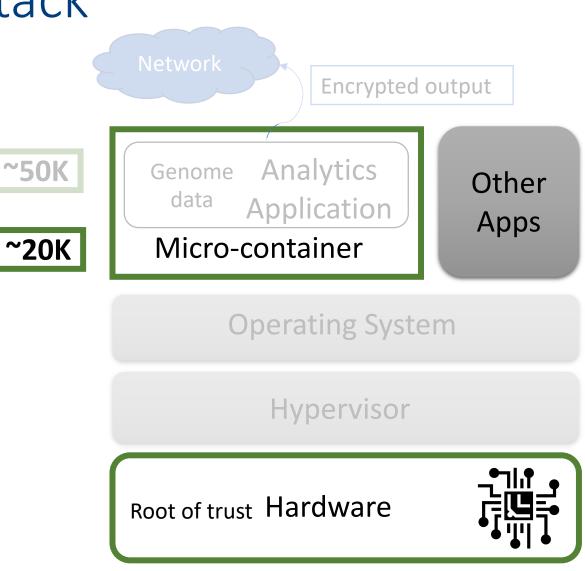
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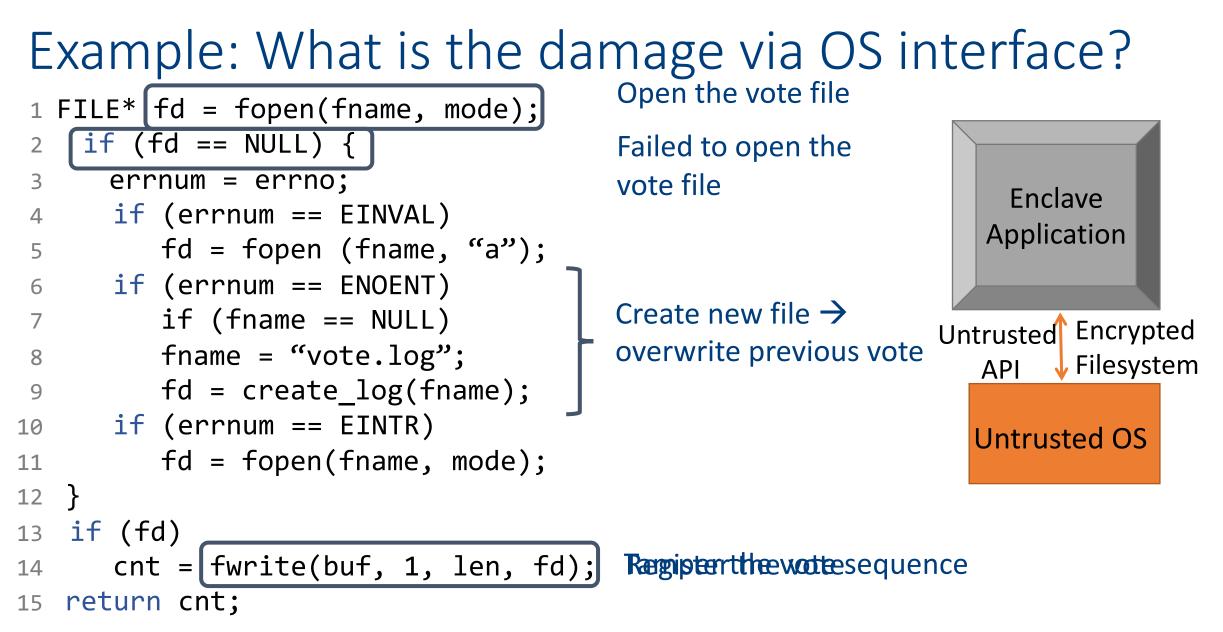
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BesFS: A POSIX Filesystem for Enclaves with a Mechanized Safety Proof [Usenix Security'20]

Attacks are possible in delegation frameworks

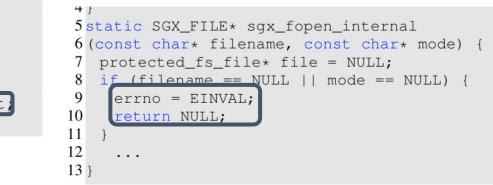
9int enc_untrusted_open(const char *path_name, int flags) {

```
10 uint32_t mode = 0;
11 int result;
12 sgx_status_t status = ocall_enc_untrusted_open(&result,
```

```
path_name, flags, mode);
13
14
15 return -1;
16
17 return result;
```

fopen: Google Asylo

```
fopen: Intel SDK
```

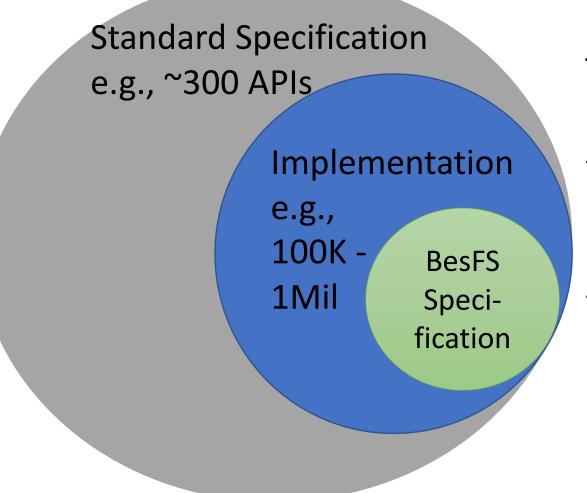


```
7 static int sgx_ocall_open(void * pms) {
8   ms_ocall_open_t * ms = (ms_ocall_open_t *) pms;
9   int ret;
10   ODEBUG(OCALL_OPEN, ms);
11   ret = INLINE_SYSCALL(open, ...);
12   return IS_ERR(ret)?unix_to_pal_error(ERRNO(ret)):ret;
13 }
```

fopen: Graphene-SGX

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A Formal Verification Approach: How to scale to POSIX?



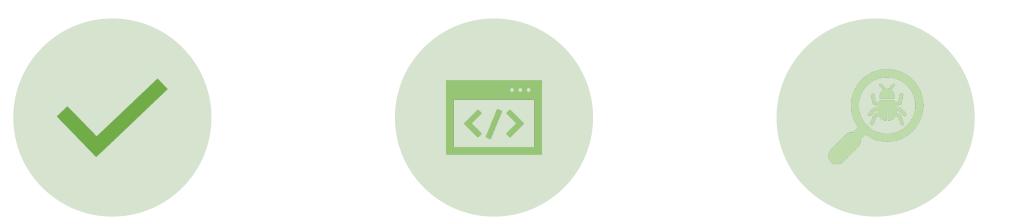
The scalability challenge:

- Specification for safe behavior for the entire POSIX API
- Proving safe implementation
 - entire libc(glibc, musl)
 - filesystem (ext4)

Designing Scalable Specification: BesFS Interface

- Our Approach
 - 15 core APIs: e.g., open, close, read, write
 - Allow to execute any sequence of these while maintaining safety property
- Can be composed to express higher-level interfaces
 - e.g., fwrite can be composed with write and fstat
 - Created 22 auxiliary APIs witnessed in applications

BesFS Highlights



4625 lines in Coq 167 lemmas (< 1.5K in C code)

Not over restrictive Supports all applications from Panoply (& more)

Total 31 tested

Helped in eliminating bugs (from Panoply, Intel SDK, Google SDK)

Towards Next Generation Computation Stack

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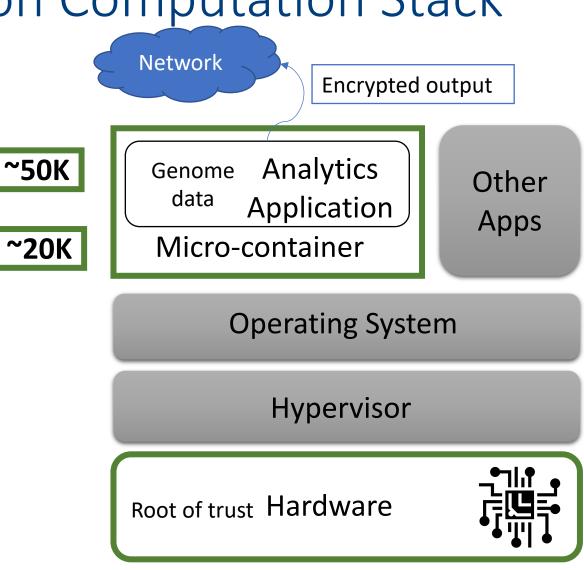
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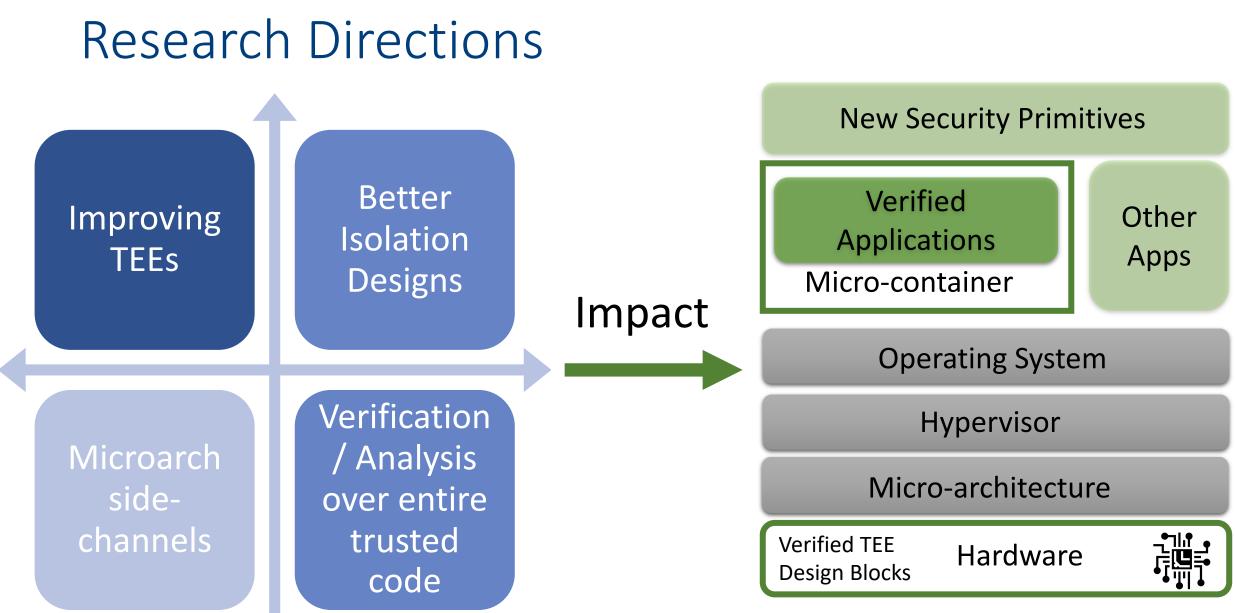
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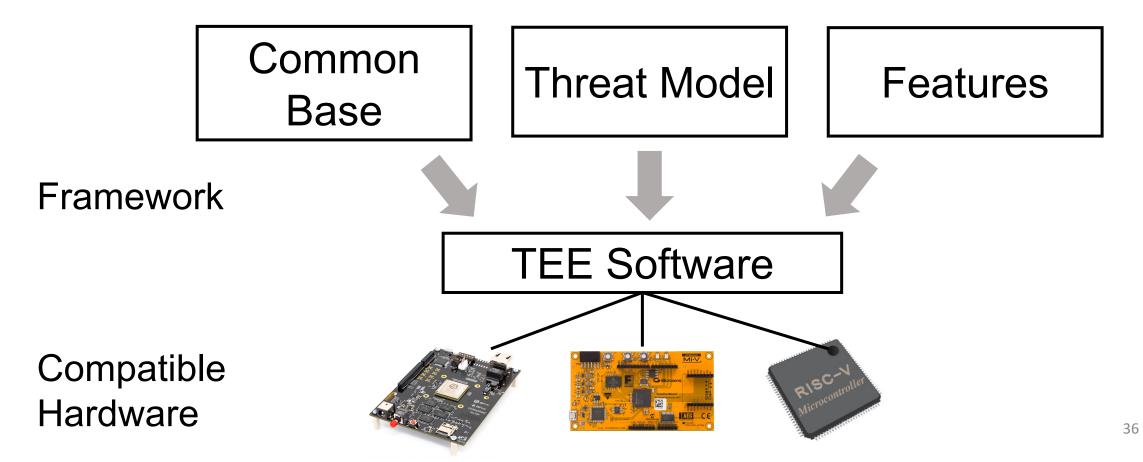
Trusted Computing Primitives [TR'15], [Eurosys'20]





Customizable TEEs

- A framework that provides building blocks of TEEs
- The platform provider and the enclave developer "customizes" the TEE



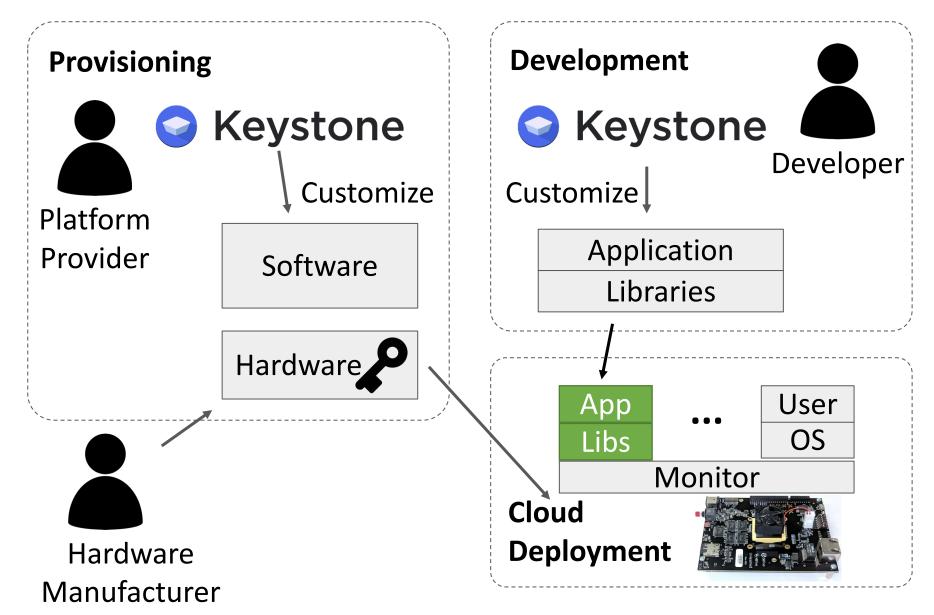


A software framework for TEEs on RISC-V

No micro-architectural changes

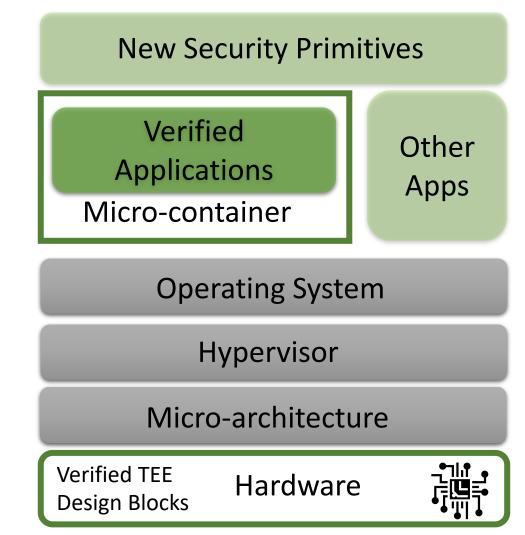
Minimal added hardware

Keystone Workflow for Customizable TEEs



Research Goals for Future TEE Platforms

- Modular TCB, easy to reduce and verify
- Binary compatibility with legacy applications
- Enable support for various backend hardware platforms
- Evolve to better hardware designs for TEE independently of the software







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